TITLE

METHOD OF FORMING GEOMETRIC DEEP TRENCH CAPACITORS

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a field emission display (FED) and fabrication method thereof, and more specifically to a triode-type field emission display (FED) having a grid plate with spacer structure and fabrication method thereof.

Description of the Related Art

With the wide application of integrated circuits (ICs), various semiconductor devices with higher efficiency and lower cost are produced based on different objectives. DRAM is important in the information and electronics industry, with memory capacity a key characteristic thereof.

Most DRAM has one transistor and one capacitor per DRAM cell. Memory capacity of the DRAM has reached 256, and even 512MB. Therefore, with increased integration, reduced size of memory cell and transistor is important in manufacture of DRAM with higher memory capacity and higher processing speed. 3-D capacitors such as a deep trench capacitor can itself reduce footprint on the semiconductor substrate, and thus, is applied to fabrication of the DRAM of 512MB and above. A traditional plane transistor covers considerable area of the semiconductor substrate, creating problems for integration. Therefore, vertical transistors are becoming popular for fabrication of memory units. One

of the most used DRAM cell arrays integrates vertical transistors with trench capacitors.

Nevertheless, as the size of elements is continuously reduced, so is trench storage node capacitance of DRAM. As a result, storage capacitance must be increased to maintain performance. Even though the storage capacitance can be increased by increasing the depth of the deep trench capacitor, finite depth limits the high aspect ratio capacitor process.

Currently, the method for increasing storage capacitance for DRAMs increases the width of the bottom of the trench, thereby increasing surface area to form a bottle-shaped trench capacitor.

FIGS. 1a to 1c are cross-sections illustrating the conventional process flow for forming a bottle trench. First, referring to FIG. 1a, a patterned pad layer 12 is formed on a silicon substrate 10. Then, the patterned pad layer 12 is used as an etching mask to etch the silicon substrate 10 by dry etching to form a trench 14 containing an upper portion 16 of width 13 and a lower portion 18.

Next, referring to FIG. 1b, a photoresist layer 22 covering the lower portion 18 of the trench 14 is formed. Subsequently, a sacrificial layer 20 covering the upper portion 16 of the trench 14 and the pad layer 12 is deposited. Then, referring to FIG. 1c, the photoresist layer 22 and the sacrificial layer 20 from the pad layer 12 are later removed by anisotropic etching. As a result, the sacrificial layer 20 is formed in the upper portion 16 of the trench 14.

Finally, referring to FIG. 1d, the silicon substrate 10 uncovered by the sacrificial layer 20 of the lower portion 18 of the trench 14 is etched by isotropic etching using ammonia and diluted hydrogen fluoride to form the lower portion 24 of the bottle-shaped trench 14. The lower portion 22 is wider (at width 15) than the upper portion 16 (at width 13).

It is difficult to control the shape of the lower portion 22 of the trench 14 by the above method, which results in increased instability and difficulty during the fabricating process.

Therefore, a manufacturing process of trench capacitor with increased storage capacitance, in which trench depth and bottom width are not increased, is called for.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide a method of forming capacitors for which the manufacturing process is simplified and storage capacitance is increased to accommodate increased integration.

Another object of the present invention is to provide a method of capacitors formation to facilitate increased storage capacitance utilizing a geometric deep trench, without increasing the width of the trench bottom.

To achieve the first object, the present invention provides a method of forming capacitors having geometric deep trenches.

First, a substrate is provided, with a pad structure and a first hard mask layer formed sequentially thereon.

Next, a patterned second hard mask layer is formed on the first hard mask layer.

Next, a spacer layer is formed in the first opening on the first hard mask layer to expose a second opening.

Next, a third hard mask layer is formed to fill the second opening, and the spacer layer is then removed.

Next, the first hard mask layer is etched to expose a third opening with a salient of the first hard mask layer, with the second hard mask layer and the third hard mask layer acting as masks.

Finally, the first hard mask layer, the pad structure, and the substrate are etched simultaneously to form a geometric deep trench in the substrate.

In the present invention, the process of etching the first hard mask layer, the pad structure, and the substrate simultaneously to form a geometric deep trench in the substrate further comprises the following steps.

First, the first hard mask layer, the salient of the first hard mask, and the substrate are etched to remove the salient of the first hard mask layer completely, and a doughnut-shaped hollow of the substrate is formed.

The doughnut-shaped hollow of the substrate and the pad structure are then etched sequentially to form the geometric deep trench.

According to one aspect of the present invention, the width of the second opening is in inverse ratio to that of the subsequently formed spacer layer.

In another aspect of the present invention, the width of the salient of the first hard mask layer is in direct ratio to that of the second opening.

The present invention also provides another method of forming capacitors having geometric deep trench, including the following steps.

First, a substrate with a pad structure s provided, wherein the pad structure comprises a pad oxide layer and a pad nitride layer formed thereon.

A first hard mask layer is formed on the substrate, followed by a patterned second hard mask layer to expose a first opening.

Next, a spacer layer is formed in the first opening on the first hard mask layer to expose a second opening.

Next, a third hard mask layer is formed to fill the second opening.

Next, the third hard mask layer is subjected to a flattening process to remove the third hard mask layer from the second opening.

Next, the spacer layer is removed completely by etching.

Next, the first hard mask layer is etched to expose a third opening with the salient of the first hard mask layer, with the second hard mask layer and the third hard mask layer acting as masks.

Next, the first hard mask layer, the salient of the first hard mask, and the substrate are etched to remove the salient of the first hard mask layer completely, and a doughnut-shaped hollow in the substrate is formed.

Finally, the hollow and the pad structure are etched to form a geometric deep trench in the substrate.

According to the present invention, the method of forming capacitors having geometric deep trench further

comprises, after etching the doughnut-shaped hollow in the substrate, the following steps.

A buried plate is formed parts of the substrate of the geometric deep trench.

A collar insulating layer and at least one conductive layer are formed in the geometric deep trench.

A detailed description is given in the following embodiments with reference to the accompanying drawings

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by reading the subsequent detailed description in conjunction with the examples and references made to the accompanying drawings, wherein:

FIGS. 1a to 1d are cross sections illustrating the manufacturing process of a conventional bottle-shaped trench capacitor.

FIGS. 2a to 2k are cross sections illustrating the manufacturing process of capacitors having geometric deep trenches in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The following embodiments are intended to illustrate the invention more fully without limiting the scope of the claims, since numerous modifications and variations will be apparent to those skilled in this art.

FIGS. 2a to 2j are cross sections illustrating the manufacturing processes of a preferable embodiment according to the present invention.

First, referring to FIG. 2a, a semiconductor substrate 100, such as a p-type silicon substrate or n-type silicon

substrate is provided. Herein, use of the term substrate includes devices formed within a semiconductor wafer and the layers overlying the wafer. Next, a pad structure 102 is formed on the substrate 100. The pad structure 102 can comprise a pad oxide layer or a pad nitride layer, wherein the pad oxide layer can be formed on the substrate in advance, and a pad nitride layer formed on the pad oxide layer subsequently. Preferably, the pad oxide layer, such as silicon oxide with a thickness of 50Å to 300Å, is formed using thermal oxidation at 850-950C°, APCVD, or LPCVD. The pad nitride layer such as silicon nitride with a thickness of 1000Å to 2000Å is formed using LPCVD at 750-800C°, wherein $SiCl_2H_2$ and NH_3 are reactants.

Subsequently, referring to FIG. 2b, a first hard mask layer 110 is formed on the ad structure 102, and a second hard mask layer 112 is formed on the first hard mask layer 110. Next, a photoresist pattern 120 is formed on the second hard mask layer 112 by photolithography. Suitable material for the first hard mask layer 110 is silicide, such as boro phosphor silicate glass (BPSG), phosphor silicate glass (PSG), boro silicate glass (BSG), or arsenic silicate glass (AsSG). Preferably, the first hard mask layer 110 of BSG with a thickness of 8000 to 15000Å, such as 13000Å, is formed by LPCVD, wherein SiH_4, BF_3, and B_2H_6 are reactants. Suitable material for the second hard mask layer 112 is polysilicon or doped polysilicon. Preferably, the second hard mask layer 112 of polysilicon with a thickness of 500 to 5000Å is formed by LPCVD at 500-650C° with doped ion concentration between 1E20 to 1E21 atoms/cm3, wherein PH_3, SiH_4, and N_2 are reactants. The

thickness of the second hard mask layer 112 can be 3000Å in this embodiment.

Subsequently, referring to FIG. 2c, the second hard mask layer 112 is etched anisotropically with the photoresist pattern 120 acting as a mask, to form a first opening 130 and expose the first hard mask layer 110. Preferably, the anisotropic etching process can be MERIE, ECR or RIE with reactants comprising SF_6, O_2, Cl_2, HBr, or a combination thereof.

Subsequently, referring to FIG. 2d, the photoresist pattern 120 is removed, and a spacer layer 124 formed conformally on the first hard mask layer 110 and second hard mask layer 112 and in the first opening 130. Suitable material for the spacer layer 124 is dielectric material such as silicon nitride, and the spacer layer 124 can be formed by a method such as LPCVD, PECVD, HDPCVD, APCVD, or SACVD.

Subsequently, referring to FIG. 2e, the spacer layer 124 is etched anisotropically, for example as RIE, to remove the spacer layer 124 from the second hard mask layer 112 and a part of the spacer layer 124 formed into the first opening 130 to form a second opening 132, by a self-aligned etching step resulting in a precise scale of the second opening 132.

Subsequently, referring to FIG. 2f, a third hard mask layer 114 is formed on the above structure to fill the second opening 132. Herein, the third hard mask layer 114 can be subjected to a flattening process to remove the part of the third hard mask layer 114 from the second opening 132. Suitable materials for third hard mask layer 114 and

second hard mask layer 112 can be the same or different. Furthermore, the materials of third hard mask layer 114 and the second hard mask layer 112 are different from those of the first hard mask layer 110. The suitable material of the third hard mask layer 114 can be polysilicon. Preferably, the third hard mask layer 114 of polysilicon is formed by LPCVD at 500-650C°. In addition, the flattening process can be chemical mechanical polishing.

Subsequently, referring to FIG. 2g, the spacer layer 124 is removed completely by, for example a hot phosphoric acid solution, to expose the first hard mask layer 110. Next, referring to FIG. 2h, the first hard mask layer 110 and the substrate 100 are etched to expose a third opening 134 with a salient 110a of the first hard mask layer 110, with the second hard mask layer 112 and the third hard mask layer 114 acting as masks. Next, the second hard mask layer 112 and the third hard mask layer 114 are removed.

Subsequently, referring to FIG. 2i, the salient 110a of the first hard mask layer 110, the first hard mask layer 110, and the substrate 100 are etched to remove the salient 110a of the first hard mask layer 110 completely, with the first hard mask layer 110 beyond the third opening 134 acting as a sacrifice layer to protect the substrate 100 under the first hard mask layer 110, resulting in a doughnut-shaped hollow 136 in the substrate 100 formed by etching of the substrate 100. When the salient 110a is removed completely by etchimg, the first hard mask layer 110 beyond the third opening 134 is etched to form a residual first hard mask layer 110b simultaneously, due to

salient 110a having a higher etching rate than the first hard mask layer 110.

Subsequently, referring to FIG. 2j, the doughnut-shaped hollow 136 of the substrate 110 and the pad structure 102 are etched by anisotropic etching such as RIE, with the residual first hard mask layer 110b acting as a mask, to form the geometric deep trench 138. Moreover, an additional sacrificial layer can be formed on the residual first hard mask layer 110b to maintain the entire sacrificial layer, comprising the residual first hard mask layer 110b and the additional sacrificial layer, has a thickness sufficient to protect the substrate 100 during the etching of the doughnut-shaped hollow 136 of the substrate 110.

Finally, referring to FIG. 2k, a buried plate 140, a collar insulating layer 150, and a first conductive layer 142 and second conductive layer 144 are formed to the geometric deep trench 138. Preferably, doped ASG and TEOS are formed into the trench 138 and heated to form the buried plate 140 by driving.

The capacitors fabricated by the method according to the present invention allow large increments of surface area and improvements of the storage capacitance for the capacitors, without the conventional complicated process on failing increased width and depth of a capacitor trench. The method of forming capacitors in accordance with the present invention solves the previously described problem resulting from the geometric deep trench of the capacitor.

Moreover, due to the decreased width of capacitor trench, it is extremely difficult to form a geometric deep

trench with precise scale by photolithography. The method of forming capacitors having geometric deep trench according to the present invention employs a self-aligned etching step to form the geometric deep trench with a salient thereinto. The self-aligned etching step allows capacitors with narrow geometric deep trench to be fabricate, even under the 0.11-Micron DRAM process.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.